# 15th MRAM Global Innovation Forum

## Hilton Union Square – room Imperial B, San Francisco

## December 14, 2023

15th MRAM Global Innovation Forum 2023 10th anniversary

IEEE MAGNETICS SAMSUNG

| SESSIONS | | TOPICS | SPEAKERS |
|---|---|---|---|
| 08:40-09:00: WELCOME & INTRODUCTION (B. Dieny, K. Garello, D. Worledge, E.S. Jung) | | | |
| EMBEDDED MRAM (chair: Daniel Worledge) | 09:00 | MRAM for Automotive Applications | Thomas Jew *NXP*  |
| | 09:30 | STT-MRAM for Automotive Grade MCU | Johannes Müller *GlobalFoundries*  |
| | 10:00 | Status and Outlook of Embedded MRAM Technology at the 14nm Logic Node and Beyond | Junghoon Bak *Samsung*  |
| 10:30-10:50 COFFEE BREAK | | | |
| STANDALONE MRAM (chair: Luc Thomas) | 10:50 | Introduction to Standalone NVRAM Based on Samsung 28nm STT-MRAM and Outlook for Standalone MRAM | Yong Hwan Noh *Netsol*  |
| | 11:20 | STT-MRAM Breaks Through Performance and Capacity Limits to Achieve Improved System Performance | Joe O'Hare *Everspin Technologies*  |
| | 11:50 | Enhancing MRAM Performance and Usability Through Innovative Memory SOC Subsystem | Jack Guedj *NUMEM*  |
| 12:20-14:00 LUNCH BREAK | | | |
| EMERGING MRAM DEVICES (chairs: Kyung-Jin Lee, Jordan Katine) | 14:00 | Demonstration of Accelerated STT-Switching and High Retention in 14nm MTJ Towards High-Density STT-MRAM | Masahiko Nakayama *KIOXIA*  |
| | 14:30 | High-Performance SOT-MRAM with 1ns Speed and 10-Year Data Retention for Cutting-edge Applications | MingYuan Song *TSMC*  |
| | 15:00 | Low Current SOT-MRAM with Brand New Mechanism for Retention Energy | Hiroaki Yoda *YODA-S, Inc.*  |
| | 15:30 | Voltage Controlled Spintronics for Memory and Stochastic Information Processing Applications | Kang L. Wang *UCLA*  |
| 16:00-16:45 BEER STUB | | | |
| PANEL DISCUSSION (Lead: Jack Guedj ) | 16:45<br>17:45 | **Magnetic Immunity: A Manageable Evil or a Show Stopper ?**<br>Bernard Dieny (*Spintec*), Sanjeev Aggarwal (*Everspin*), Yoon Jong Song (*Samsung*), Biay-Cheng Hseih (*Qualcomm*), Johannes Müller (*GF*), Thomas Jew (*NXP*)  | |
| 17:45 Closing remarks | | | |

## MRAM for Automotive Applications

### Thomas Jew, *NXP*

Thomas Jew is a Fellow in NXP's CTO, Front End Innovation group and currently leads Non-Volatile Memory development for Advanced Microcontroller and Microprocessor applications. He has worked on discrete non-volatile memory products and embedded memory designs including traditional flash and disruptive memory technologies integrated in microcontrollers for IOT and automotive applications for ~29 years. Prior to joining NXP by way of Freescale Semiconductor/Motorola, he worked for Texas Instruments, designing discrete flash memories. Thomas received his BS and MS degrees in Electrical Engineering from Texas A&M University in 1988 and 1991 respectively.

**Abstract:** MRAM is establishing itself as a viable non-volatile memory (NVM) solution for advanced Microcontrollers. In particular, the industry is seeing a number of devices with embedded MRAM running in production for consumer applications in 2x nodes. This progress is helping to pave the way for integrating MRAM into Automotive Applications. This talk will focus on why now is the right time to integrate MRAM into Automotive Applications, and why embedded MRAM is key for enabling next generation Automotive Applications such as Zonal and Domain controller architectures, and how MRAM can help drive the evolution to realizing the Software Defined Vehicle.

## STT-MRAM for automotive grade MCU

### Johannes Müller, *GlobalFoundries*

Dr. Müller is currently leading the MRAM stack development in the T&D Organization of GlobalFoundries. Previously, he was acting as the overall-integrator for the now qualified and volume-ramped 22FDX® embedded STT-MRAM technology. Prior to joining GlobalFoundries, Dr. Müller headed the group for Non-Volatile Memories at Fraunhofer society overseeing direct industry collaborations and EU projects focused on FRAM, FeFET, STT-MRAM, OXRAM, and eFLASH. With the discovery of ferroelectricity in HZO and the first demonstration of a FeFET scaled to the 2X nm node Dr. Müller largely contributed to the recent revival of ferroelectric memories and devices.

To date Dr. Müller has (co-)authored >150 peer-reviewed journal and conference papers and holds several patents (Hirsch-index: 50). As panelist, invited speaker and short course tutor, Dr. Müller has served the scientific community at e.g. IEDM, IMW, NVMTS, SSDM, SISC, INTERMAG, etc., and, as an expert in his field, contributed to the ERD Working Group of the former ITRS.

**Abstract:** With a broad industry consensus STT-MRAM has successfully entered the embedded NVM market at the 2X nm node. This first entry point as an eFLASH replacement is mainly focused on microcontroller units (MCU) targeted for low-power consumer/industrial Internet of Things (IoT) applications. However, with the now rapid acceleration of fully electrified mobility and autonomous driving on the horizon, the automotive sector projects a growing need for more performance and cost-effective chip solutions. Due to the fading scalability roadmap of the highly trusted eFLASH technologies, a new, robust, and reliable NVM solution must be established to serve the needs of future automotive nodes. Through its consumer-/industrial-grade qualification and volume ramp, STT-MRAM has proven to be the most reliable amongst the former emerging memories and can be viewed as the predestined successor of eFLASH in this demanding application space. In addition to its superior scalability, STT-MRAM offers higher write speed and cycling endurance compared to its predecessor. Especially for fast Over-The-Air (OTA) updates and functionality beyond code-storage, such as data-logging, these new features are highly attractive.

In this talk, we will review the challenges and required MTJ stack innovations on the road towards an automotive capable embedded STT-MRAM solution.

Due to the multitude of individual microchips in a modern vehicle whose malfunction could ultimately lead to a critical error, the chip failure rate (CFR) per each individual component needs to be strongly reduced. To keep enough reliability margin for the error correction code (ECC) at the end of life (EoL), the initial bit error rate (BER) needs to be pushed to the deep sub-ppm regime. Achieving this for cross temperature (-40°C to 150°C) readability and write error rate (WER) requires significant advancements from the first generation of embedded STT-MRAM.

## Status and outlook of embedded MRAM Technology at the 14nm Logic Node and Beyond


### Junghoon Bak, *Samsung*


Dr. Junghoon Bak is Principal Engineer of the advanced technology development team in Samsung semiconductor R&D center, where he is engaged in the development of MRAM technology. He received his Ph.D and BA degree in Physics from Seoul National University. Since joining Samsung Electronics in 2009, he has been involved in the development of various new memory technologies such as MRAM, PRAM and DRAM. He has particularly focused on developing new integration processes as well as on the measurement and analysis for next generation memory.


**Abstract:** Spin transfer torque based magnetic random access memory (STT-MRAM) has been receiving growing attention due to great compatibility with logic processes and excellent performance as the next-generation embedded non-volatile memory solution. In 2019, Samsung Electronics Co., Ltd. began mass production of the world's first eMRAM using the 28nm logic process. We are currently developing eMRAM for Consumer, Industrial, and Automotive applications at the 14nm and beyond technology nodes by improving the process to expand operating temperature and application range. Here, at first, we demonstrate successful development of a highly reliable and manufacturable embedded MRAM macro for automotive application in 14nm FinFET logic platform through advanced MTJ stack and innovative novel process integration scheme. In the case of automotive eMRAM, high operating temperature up to 150 C and high reliability with endurance over $10^6$ cycles and 10 years retention at 150 C are required. To operate at high temperatures, it is necessary to improve the thermal stability of the magnetic film, which has been achieved by introducing a novel thin film technology that enhances the crystallinity. Based on these improvements, the full functionality of write and read operations at temperature ranging -40°C ~ 150°C was achieved with stable yield up to 90% while satisfying critical reliability characteristics. These results prove the potential for automotive application of our eMRAM technology. Subsequently, we also present the current status of the technological advancements in eMRAM development for sub logic nodes below 10nm.


## Introduction to standalone nvRAM based on Samsung 28nm STT-MRAM and outlook for standalone MRAM


### Yong Hwan Noh, *NETSOL*


Yong Hwan Noh is SVP and CTO of Netsol, a global provider of standalone MRAM and SRAM products. He worked as a principal design engineer for SRAM and DRAM in Memory Division of Samsung Electronics for 14 years. He has led the development of Netsol's SRAM products. Currently, he is focusing on developing MRAM products. Recently, Netsol has launched its first MRAM products. He received M.S. in Electrical Engineering and B.S. in Physics from Pohang University of Science and Technology, South Korea, in 1997 and 1995 respectively.


**Abstract:** The standalone MRAM product, first commercialized as Toggle MRAM, has a history of about 15 years and its market is further expanding with STT-MRAM technology. STT-MRAM has been

replacing traditional memories such as FeRAM, nvSRAM and Low-power SRAM, and adopted to various applications such as smart meter, PLC, industrial automation, gamming, RAID, robotics, and so on. STT-MRAM products with higher densities are expected to expand to even more applications.

Netsol has recently completed the development of its first standalone STT-MRAM products (SPI, PPI, 1Mb~32Mb) using 28nm eMRAM technology from Samsung Foundry. In this talk, we will introduce the features of these products and extensive test results such as endurance, data retention, magnetic field immunity and qualification. We will also talk about the outlook of future standalone STT-MRAM products.

## STT-MRAM Breaks Through Performance and Capacity Limits to Achieve Improved System Performance

### Joe O'Hare, *Everspin Technologies*

Joe has had a rewarding career working in the semiconductor industry at companies such as TI, Lucent Microelectronics, Agere Systems and now Everspin Technologies. He has held a variety of engineering, marketing and executive positions with a focus on developing products for the storage industry, both magnetic and solid state. These include Storage Business Unit Director at Lucent and EVP of the Storage Business at Agere Systems.

At Everspin Technologies, Joe has held roles in sales and marketing since 2011. As Sr. Director of Marketing at Everspin Technologies, Joe is leading the effort to define and launch a new class of STT-MRAM memory that is targeted at storage and industrial applications where performance and persistence are valued. Joe has overseen the product launch of 5 generations of MRAM products, most recently with the 28nm family of xSPI for the Industrial and IoT market, solidifying the company's leadership in the commercialization of MRAM technology.

**Abstract:** Industrial electronics systems are becoming increasingly complex with the adoption of AI processing, high speed connectivity, and deployment in harsh environments. In this talk we will show how the versatility of STT-MRAM technology provides system improvement through optimization for different memory workloads. STT-MRAM process and design architecture play key roles in attaining performance and reliability levels needed for the memory requirements of embedded computing systems. Enabling customers with standard interface and packaging makes the adoption of STT-MRAM products a straightforward design-in process. New advances are coming on the near-term roadmap for 1 Gigabit products with enhanced performance over alternative non-volatile memories.

## Enhancing MRAM Performance and Usability through Innovative Memory SOC Subsystem

### Jack Guedj, *NUMEM*

Jack was President and CEO of Tensilica since 2008 where, he transformed Tensilica into a rapidly growing company ascending to the #1 position in merchant DSP and ultimately leading to the Cadence acquisition in 2013 where he served as Corporate VP, Tensilica Products.

Prior to Tensilica Jack led the spin-out of Magnum from Cirrus Logic serving as founder, president and CEO. Jack led Magnum's growth from ground zero to leadership in Multimedia SOCs for the Professional Video Broadcast, Consumer PVR TV/Camcorder/DVD Recorder and Set Top Box markets and the acquisition of the Consumer Products Group of LSI Corporation (C Cube). Prior to Cirrus, Jack was President of Tvia, Inc., leading that company's successful IPO in August 2000. Jack holds an MBA from the UCLA Graduate School of Management. Jack attained a MSEE from Pierre & Marie Curie Engineering School of Paris, and a doctoral degree from the University of Pierre & Marie Curie.

**Abstract:** This paper explores the challenges associated with MRAM, highlighting its advantages in power and area efficiency while addressing limitations in endurance, read and write speeds compared to SRAM. The presentation focuses on Numem's patented architecture solutions, demonstrating how a dedicated Memory SOC Subsystem can notably enhance Performance, Endurance, Power efficiency, and ease of use, along with improvements in Built-In Self-Test (BIST) capabilities. The proposed advancements aim to overcome existing hurdles and promote the wider adoption of MRAM technology.

## Demonstration of Accelerated STT-Switching and High Retention in a 14nm MTJ towards High-Density STT-MRAM

### Masahiko Nakayama, *KIOXIA*

Masahiko Nakayama received the Ph.D. degree in Physics from the Tohoku University, Japan, in 2002. He received B.S. and M.S. degrees in Physics from the Tohoku University, Japan, in 1997 and 1999, respectively. In 2002, He worked as an assistant in Tohoku University. In 2003, He joined the TOSHIBA Corporation. as a researcher in the Research and Development Center. In 2019, He joined the KIOXIA Corporation.

Since 2003, He has been worked on MRAM development project. He is currently a technology leader of Advanced MRAM project in the KIOXIA Institute of Memory Technology Research & Development. His research interests include MRAM device designs, MTJ designs, and electric evaluation for Advanced MRAM.

**Abstract:** Latest innovative technologies like AI, IoT, and deep learning increase demands for high-speed non-volatile memory with much higher density and lower cost as compared to conventional DRAM. STT-MRAM using perpendicular magnetic anisotropy is a promising candidate for high-density standalone-MRAM. In this talk, we introduce a novel 14nm MTJ design and demonstrate high retention and high-speed writing simultaneously towards 1Z (15-14) nm STT-MRAM. Key design concept of our MTJ, called as AccelHR-MTJ (Accelerated STT-Switching and High-Retention MTJ), is to assign the functions of high retention and high-speed writing to separate magnetic layers in a storage layer. We demonstrate excellent performance such as high retention of >10 years at 90℃, high-speed writing at 5ns pulse in our 14nm AccelHR-MTJs as predicted by its design concept. Furthermore, large Hc of 4kOe for strong magnetic immunity, large TMR ratio of 100% with low RA of 1.7Ωμm2 for large read margin, and large Hex of 14kOe in SAF for stable STT switching were successfully achieved.

## High-Performance SOT-MRAM with 1ns Speed and 10-Year Data Retention for Cutting-Edge Applications

### MingYuan Song, *TSMC*

MingYuan Song is a technical manager at Taiwan Semiconductor Manufacturing Company, with a keen interest in the field of Physics and engineering. Graduating from National Taiwan University, MingYuan's passion for the subject led him to pursue a career in SOT-MRAM technology. As a technical manager, MingYuan is currently in charge of a project dedicated to improving the performance of SOT-MRAM and exploring new applications for the technology.

**Abstract:** The rapid development of artificial intelligence in recent decades has been continuously driving new software and hardware advancements. High-dimensional matrix-vector multiplication (MVM) is a crucial component in signal processing and machine learning computations. To achieve MVM, the 2D crossbar array of memristors has been widely discussed and studied. In this work, a novel SOT-MRAM device structure with 1ns write speed and >100x scalable resistance and read current are

demonstrated to address the persistent problems of the traditional 2D crossbar array, leveraging its read-write path separation nature.

## Low Current SOT-MRAM with Brand New Mechanism for Retention Energy


### Hiroaki Yoda, *YODA-S, Inc.*


Hiroaki Yoda is CEO & CTO at YODA-S, Inc. since 2019. Previously, he was senior fellow at Toshiba & Kioxia (-2018) and MRAM leader (2001-2013) at Toshiba. He led various government projects such as Field-writing MRAM, Spin-RAM, Normally-off Computing and ImPACT. He has been awarded by Japanese invention commendation, Ichimura Industrial award, Nikkei BP Grand award and Toshiba President award.


**Abstract:** Memory hierarchy consists of volatile cache memories and non-volatile storage because non-volatility and low power do not coexist in one memory device. For coming AI applications, the current memory hierarchy has issues with narrow bandwidth of data transfer rate and huge energy consumption. A roadmap of essential solutions to the issues is shown in Fig.1. YODA-S, Inc. has faced the challenge along this tough road.

In this talk, 1st, the final goal of in-memory computing is explained. 2nd, the root cause of the no coexistence is addressed. 3rd, MRAM's inherent potential to solve the root cause is explained. Finally, the progress of SOT-MRAM using MTJs with strain-induced magnetic anisotropy (SIMA-MTJs) is reported and it is concluded that the new SOT-MRAM has a potential to have the coexistence as shown in Fig.2.


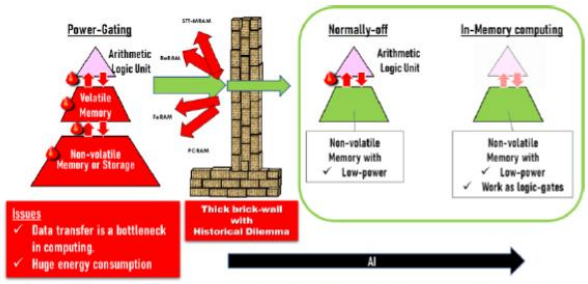


Fig. 1 Essential solutions for the current memory hierarchy.

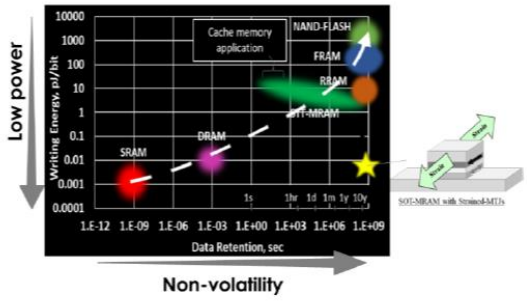


Fig. 2 Expected low power of SOT-MRAM with SIMA-MTJs

## Voltage Controlled Spintronics for Memory and Stochastic Information Processing Applications


### Kang L. Wang, *University of California, Los Angeles*


Dr. Kang L. Wang is currently a Distinguished Professor and the Raytheon Chair Professor in Physical Science and Electronics at the University of California, Los Angeles (UCLA). He is affiliated with the Departments of ECE, MSE, and Physics/Astronomy. He is also the Co-Director of the UCLA Quantum Science and Engineering and the Director of the Joint Center of Green Nanotechnology – between UCLA and the King Abdulaziz City for Science and Technology, Saudi Arabia. He received his M.S. and Ph.D. degrees from the Massachusetts Institute of Technology and his B.S. degree from National Cheng Kung University (Taiwan). He was with HKUST as a Professor and the Dean of School of Engineering from 2000-2003. Previously, he also served as the Chair of Electrical and Computer

Engineering of UCLA from 1992-1996. His research areas include semiconductors, topological matters, spintronics/magnetics, nonvolatile electronics, and quantum information and computing.

**Abstract:** Spintronics provides an energy-efficient high-speed nonvolatile approach for next-generation memory and information processing applications to complement CMOS technology. Among many spintronic devices include those based on spin-transfer torque, spin-orbit torque, and voltage-controlled magnetic anisotropy. We will describe voltage-controlled magnetic anisotropy (VCMA) magnetic memory, which has been demonstrated to achieve among the lowest switching energy. Next, we will discuss voltage-enabled Dzyaloshinskii-Moriya Interaction (DMI) for additional functionalities. Then, the talk will discuss the challenge in integration of VCMA on CMOS, in particular with respective of maintaining VCMA coefficient and TMR demonstrated in laboratory in a lab-to-fab effort. The electric field control of VCMA (and DMI) may be further used for important computational applications, for example, in stochastic computing and other computation-in-memory systems. However, major challenges remained to be resolved for realizing high-density memory and high marketing-level applications. Among the needed is a high TMR (on-off ratio); continuously increasing VCMA and voltage-controlled DMI coefficients will also be required to greatly improve the scaling of device density and system performance. The uniqueness of stochasticity of spintronics via voltage control may offer new opportunities for additional application areas.

## PANEL DISCUSSION:

# Magnetic Immunity: A manageable evil or a show stopper?

## Moderator: Jack Guedj (Numem)

### Yoon Jong Song, *Samsung*

Dr. Yoon Jong Song is VP and head of Advanced Technology Development Team in Samsung R&D Center, leading the development of STT-MRAM and emerging memory such as SOM (selector only memory). He is mainly involved in process integration and device characterization for 14nm/8nm eMRAM. Since he joined Samsung Electronics in 1998, he has experience of developing various new memories including FRAM, PRAM, and MRAM. His specialty is to integrate new memory devices and to establish new characterization method and reliability standards. He has authored or co-authored over 100 publications related to new memory fields.

### Bernard Dieny, *Spintec*

Dr. Bernard Dieny has been conducting research in magnetism and spin electronics for 35 years. In 2001, he launched SPINTEC laboratory (Spintronics and Technology of components) in Grenoble and cofounded two startup companies in 2006 and 2014. He received two Advanced Research grants from the European Research Council in 2009 and 2014 related to hybrid CMOS/Magnetic Integrated Electronics. He was nominated IEEE Fellow in 2010, received the De Magny Prize from French Academy of Sciences in 2015 and the IEEE Magnetics Society Achievement

Award in 2019. His field of expertise covers a broad spectrum from basic research in nanomagnetism and spin-electronics to functional spintronic devices, in particular MRAM. In 2009, he also launched an activity merging nanomagnetism and biology with a particular focus on magnetically induced mechanical stimulation of living cells with potential applications for innovative treatments of cancers, diabetes and neurodegenerative diseases.

## Sanjeev Aggarwal, Everspin

Dr. Sanjeev Aggarwal serves as a member of our Board of Directors and as President and Chief Executive Officer of Everspin. With over 25 years of expertise in the non-volatile memory and semiconductor industry, Sanjeev has been instrumental in shaping Everspin since its inception in 2008 through various leadership positions. Most recently, he served as the Chief Technology Officer driving product and technology roadmaps and business agreements with partners, vendors, and suppliers. As the Vice President of Technology R&D, he directed cross-functional teams to develop and qualify innovative technology and products. As Vice President of Operations, he managed manufacturing operations, supply chain, and managed joint development agreements for technology transfer and production. Before Everspin, Sanjeev was at Freescale Semiconductor and part of the team that spun out to form Everspin Technologies.

Prior to his work on MRAM, Sanjeev successfully developed and commercialized Ferroelectric memories at Texas Instruments. In 2005, he was awarded the Technical Excellence Award by the International Symposium on Integrated Ferroelectrics for his contributions to commercializing FRAM technology. Sanjeev is Senior Member of IEEE, and his technical contributions include over 200 issued patents, more than 100 publications and numerous invited presentations. He graduated from Cornell University with a doctorate in Materials Science and Engineering and received his bachelors from Indian Institute of Technology, Varanasi in Ceramic Engineering.

## Biay-Cheng Hseih, *Qualcomm*

Biay-Cheng Hseih received his Ph.D. degree in electrical and computer engineering from Carnegie-Mellon University at Pittsburgh, PA, USA, in 1989. He is currently an Engineering Principal/Manager in Multi-Media Research and Development Group, Qualcomm Technologies, Inc. San Diego. Prior to joining Qualcomm, in 2013, he has been with TSMC R&D Division, Conexant System/Rockwell Semiconductor System, and Kodak, on diverse projects including CMOS image sensor, CCDs, and low-temp poly-Si TFT OLED display in device engineering, detector array technology development, imager analog front-end noise cancellation readout chain designs, image characterization, and human vision camera technologies. His current R&D projects are focused in the areas of Machine Visio Sensing and Processing Engine prototype design/development, and 3D Depth computational Camera Technologies development.

## Johannes Müller
## GlobalFoundries

## Thomas Jew
## NXP

Bio in speaker section


1st Forum : San Jose, California
2nd Forum: Tokyo, Japan
3rd Forum : Paris, France
4th Forum : Seoul, South Korea
5th Forum: Tokyo, Japan
6th Forum: Santa Clara, California
7th Forum: Zurich, Switzerland
8th Forum: Seoul, South Korea
9th Forum: San Francisco, Dec. 2017
10th Forum: San Francisco, Dec. 2018
11th Forum: San Francisco, Dec. 2019
12th Forum: Virtual, joint with Intermag21, Ap. 2021
13th Forum: San Francisco, Dec. 2021
14th Forum: San Francisco, Dec. 2022

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