IEDM 2023 Special MRAM poster session

Tuesday Dec. 12th,2:20pm - 5:30pm

Yosemite room

A special poster session entirely dedicated to MRAM is organized during IEDM. This session is technically organized by the IEEE Magnetics Society and embedded in the IEDM 2021 conference. This event will be a great opportunity to foster closer interactions between the microelectronics and magnetism communities. The poster session will cover a number of topics including MRAM materials, phenomena, technology (STT, SOT, E-field control), testing, hybrid CMOS/MTJ.

Posters abstracts:

1. Perspectives Field-Free, 2-Terminal SOT-MRAM at Deeply Scaled Technology Nodes with 1x nm MTJ Critical Dimension

William Hwang[1], Fen Xue[1], Wilman Tsai[2], Shan X. Wang[1,2]

Departments of [1]Electrical Engineering and [2]Materials Science & Engineering, Stanford University

Spin Orbit Torque (SOT) Magnetoresistive Random Access Memory (MRAM) and its variants have emerged as a promising candidate for use in SRAM-replacement applications (e.g., last layer cache, buffer memories, etc.) owing to its sub-nanosecond switching performance and favorable write-endurance properties. In this poster, we investigate 2-terminal SOT-MRAM as one such technology that promises higher bit-cell density compared to conventional 3-terminal SOT-MRAM. In conventional SOT-MRAM devices, the areal-density is constrained by the dual transistor bitcell design, as well as the need to supply a magnetic field to assist switching in perpendicular magnetic tunnel junctions (MTJs). We seek to overcome these challenges by adopting a 2-terminal device structure, with one transistor per MTJ, in order to improve the areal density of the SOT-MRAM device while leveraging spin transfer torque (STT) to break the symmetry between the parallel and antiparallel states. In a 2-terminal SOT-MRAM device, the MTJ and SOT line are connected in series, where SOT and STT are generated simultaneously when a write current is injected into the bitcell. We study 2-terminal SOT-MRAM devices with both perpendicular and in-plane magnetic anisotropy using micromagnetic simulation, and find that in-plane magnetic anisotropy presents a promising scaling pathway towards 1x nm MTJ critical dimension.

2. Spin mixing conductance at interfaces of TI/FM and HM/FM heterostructures

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The spin mixing conductance is an important figure of merit for spin transport across an interface. This is a particularly important number for Spin Orbit Torque Magnetic Random Access Devices, where spin generated in one layer is used to provide the spin torque needed to flip the magnetization in an adjacent layer. Here the spins are generated in either an topological insulator (TI) or an heavy metal (HM). The overall efficiency of such a device depends on both the charge to spin conversion in the spin generation layer and the spin mixing conductance of the interface. Here we are going to show the results on TI/FM and HM/FM interfaces. In the topological insulator the spins are generated by the spin-momentum locked states in the topological surface states, whereas in the heavy metal the spins are generated through the spin Hall effect. We will show the spin mixing conduction of several heterostructures using a variety of measurements, that include MOKE, FMR, ST-FMR, 2nd Harmonic Hall and ISHE measurements.

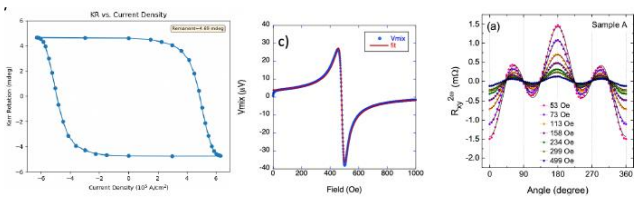

Figure 1: a) Field free switching of NiFe at RT tracked by Kerr microscopy, b) spin-torque FMR measurements show both field like and damping like SOT, c) Angle dependent second harmonic Hall data showing charge to spin conversion efficiency.

3. Enhanced spin current generation near magnetic transition in amorphous cobalt silicide

Jason Cheng-Hsiang Hsu[1,2,†], Hannah Kleidermacher[1], Emma Blenkinsop[1], Jonathon Webster[1], Shang-Lin Hsu[1], Shehrin Sayed[1,2], Alpha T. N'Diaye[3], Frances Hellman[2,4,5], Sayeef Salahuddin[1,2]

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Spin current material research has been an ongoing effort for developing energy efficient spin-orbit torque MRAM devices. To reduce the spin-orbit torque switching current, not only high spin-torque efficiency is important ($\xi_{SOT} > 1$) but also high conductivity is required for the spin current material [1]. Recently, large spin-orbit torque ($\xi_{SOT} > 1$) has been observed in fully amorphous iron silicide [2]. While the concentration dependence of spin-orbit torque in iron silicide can potentially arise from the change in density of states near the Fermi level, the role of magnetism in magnetic element silicide has not been fully understood. Moreover, the spin Hall conductivity (σ_c) in amorphous iron silicide is still lower than the best performing heavy metal candidates due to its higher resistivity. Here, we report large spin-orbit torque in fully amorphous cobalt silicide through in-plane harmonic Hall measurement. We observed that the peak efficiency of spin-orbit torque aligns with the transition of the magnetic phase, shifting from non-ferromagnetic to ferromagnetic characterized through x-ray magnetic circular dichroism. Furthermore, the high spin-orbit torque efficiency ($\xi_{SOT} \sim 2$) is accompanied by a threefold reduction in resistivity compared to amorphous iron silicide. Consequently, this leads to a spin Hall conductivity exceeding that of top-performing heavy metals like Pt and IrMn. Our discovery of an enhanced spin current near the magnetic phase transition in amorphous cobalt silicon suggests a novel approach to generating and understanding spin current in amorphous magnetic element silicide systems. This notable spin Hall conductivity makes it a silicon-compatible material suitable for efficient spin-orbit torque MRAM applications.

[1] B. Dieny, I. L. Prejbeanu, K. Garello, *et al.*, Nature Electronics, vol. 3, p. 446–459 (2020)

[2] Cheng-Hsiang Hsu, Julie Karel, Niklas Roschewsky et al. Large spin-orbit torque generated by amorphous iron silicide, 17 September 2022, PREPRINT (Version 1) available at Research Square [https://doi.org/10.21203/rs.3.rs-1946953/v1]

4. Investigation of endurance failures in SOT-MRAM devices

C. P. Jiang[1], J. H. Li[1], H. C. Zhang[1], S. Y. Lu[1], Z. K. Zhang[1], H. Zhang[1], H. Jin[1], G. F. Wang[2], H. X. Liu[2], K. H. Cao[1], Z. H. Wang[1], W. S. Zhao[1]

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Spin orbit torque (SOT) magnetic random access memory (MRAM), benefiting from the separated write and read paths, has forecasted unlimited endurance performance and ultrafast writing speed in sub-ns level [1]. Research institutions have reported [2,3] high endurance in isolated SOT-MTJs with example such as the study done by Xu et al. [3] demonstrating high endurance up to 10^{12} cycles. However, very limited array-level data have been reported for the SOT-MRAM[4,5]. Notably, there has been a pioneering effort by Van Beek et al. [4] from IMEC to study the array-level endurance for the SOT-MRAM. Their finding shows the $t_{63\%}$ lifetime of approximately 108 cycles when stressed under 100 ns pulse width. The relatively low endurance was attributed to Fe and oxygen atoms diffusion within the SOT-MTJs during the write cycles. It is clear that the reported array-level data do not align with the performance of isolated SOT-MTJ devices. In order to clarify the primary factor influencing the intrinsic endurance of the SOT-MRAM, we investigated systematically the endurance of the fabricated SOT-MRAM multiplexer (MUX) array, with an analysis of the failure mechanism. Fig. 1(a) illustrates a SEM image of a typical fabricated MTJs within the array, with the MTJ dimensions of 300×1050 nm in an elliptical shape. The SOT channels are patterned to a dumb-bell shape, with a width of 1200 nm and a length of 2500 nm. Endurance tests were conducted under accelerated bias voltage conditions, exceeding three times the critical switching voltages. The endurance performance of the SOT-MRAM was

checked under various write pulse widths, temperatures, MTJ critical dimensions, SOT channel lengths/widths, and integration processes. One of the main findings in our work, displayed in Figs. 1(b) and (c), reveals that RAP and RP remain stable even after 10^{10} write cycles at room temperature, without apparent degradation. Although the testing did not extend beyond 10^{10} cycles due to time limitations, the fabricated SOT-MRAM exhibited high endurance performance, suggesting the potential to go unlimited cycles. This result is different from the published report [4,5], which has lower endurance performance explained by the atom intermixing due to heat generation during the writing pulse. It is essential to note that our MTJ sizes are much larger than those in aforementioned report. If tested under the same current, our devices would generated more heat, given their dimensions. However, no endurance failures were observed, indicating the absence of atom interdiffusions happened, possibly because heat dissipation faster than the smaller MTJ and/or SOT channel dimensions. To further explore endurance, the test condition was changed from 25℃ to 125℃, and the write bias voltages were increased to accelerate the failures of the MTJs. Under these conditions, we observed that both the RP and the RAP, along with the tunneling magnetoresistance (TMR) decrease with increasing write cycles, as shown in Fig. 1(d). The extrapolated fitting results show that the write cycles of our SOT-MRAM can reach up to 10^{15} at 125 ℃ under the operating voltage (Fig. 1(e)). The cross-section transmission electron microscopy (TEM) image of the failed MTJ shows severe intermixing within the MTJ devices. The energy-dispersive X-ray spectroscopy (EDS) analysis shows that O, Mg, Fe, Co, Ru and other elements have different degrees of diffusion. The diffusions of atoms reduced the barrier height of MgO and the spin polarizability of the ferromagnet electrodes, leading to the decrease of TMR. Our work confirmed that the heat generated by the bias voltages dominates the endurance failure in the SOT-MRAM, which is different from that of the MgO breakdown happened in STT-MRAM case. As such, reducing the switching current or power becomes critical engineering challenge for the SOT-MRAM for the real applications.

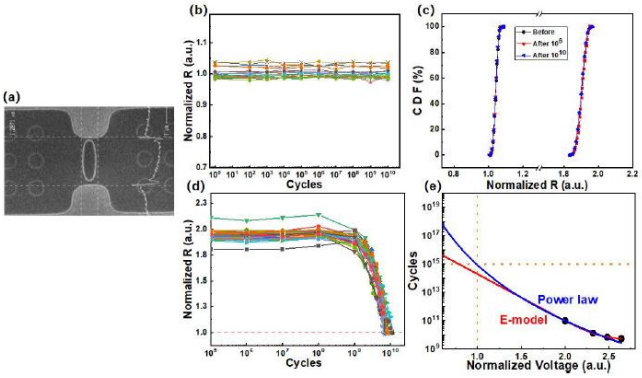

Figure 1. (a), Typical SEM images of the fabricated SOT-MTJs in Kb-level array. (b) Endurance of array devices after 10^{10} cycles and (c) the CDF diagram before (black) and after (blue) writing 1010 at 25℃. (d) The changes of MTJ resistance with the increase of write pulse cycles and (e), the endurance of the array devices can reach 1015 at the operating voltage at 125℃.

[1] Q Shao, P Li,L Liu, et al. *IEEE Transactions on Magnetic*s, 2021, 57 [2] H Zhang, X Ma, C Jiang, et al. *Journal of Semiconductors*, 2022, 43 [3] X Xu, C Jiang, H.Zhang et al. *IRPS*, 2023 [4] S Van Beek, K Cai, S Rao, et al. *IRPS*, 2022, [5] S Van Beek, K Cai, K Fan, et al. *IRPS*, 2023.

5. Selective operations of multi-pillar SOT-MRAM for high-density and low-power embedded memories

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Spin-orbit torque magnetoresistive random access memory (SOT-MRAM), featuring distinct paths for writing and reading operations, emerges as a promising candidate for L1/L2 cache SRAM replacement due to non-volatility, sub-nanosecond switching, and excellent endurance (~10^{12} cycles) [1,2]. However, the 3-terminal configuration requires at least two transistors for operation, thereby restricting integration density. In addition, the high SOT switching current of SOT-MRAM negatively impacts reliability and bit-cell density [3]. To overcome these challenges, in this contribution, we propose and demonstrate a concept of multi-pillar SOT-MRAM to enhance writing current efficiency and integration density through bit-selective read/write operations. Our devices, incorporating top-pinned perpendicular magnetic tunnel junction (MTJ) with a free layer based on CoFeB/MgO, comprise multiple MTJs with individual

top electrodes. These MTJ pillars share a common SOT track composed of W.

Typical square TMR hysteresis loops of each individual MTJ pillar as functions of field and SOT switching current indicate good uniformity regarding their locations on the track. First, we assess the influence of gate voltage (V_g) on the modulation of magnetic anisotropy (B_k) and consequently switching current through the VCMA effect [3]. From the dependence of B_k as a function of gate voltage V_g, the VCMA coefficient can be estimated as ~15 fJ/Vm [4]. Furthermore, varying gate voltages reveal that as the gate voltage increases, the critical SOT switching current decreases at a slope of ~80 µA/V, while the device sustains ultrafast switching down to 0.3 ns. Finally, we demonstrate voltage-gated selective operation in a device with two MTJs which involves achieving successful switching in the chosen MTJ while simultaneously preserving the magnetization states of the unselected pillar. As the switching probability of a positive voltage-gated MTJ shifts to a lower current while that of a negative gated shifts to a higher region, the plateau of joint switching probability on these two pillars defines the working window for selective operation.

In conclusion, our demonstration of selective operation in the multi-pillar SOT-MRAM not only reduces the number of transistors per bit but also achieves a 30% reduction in operation current. Our devices are fabricated in imec's 300 mm CMOS fab which clears the path for high-density and low-power embedded memories.

[1] K. Garello et al., *IEEE Symp. on VLSI Circuit*, 81-82 (2018).
[2] K. Cai et al., *IEEE Symp. on VLSI Circuit*, 375-376 (2022).
[3] S. Van Beek et al., *IRPS*, pp. 1-7 (2023).
[4] Y.C. Wu et al., *Phys. Rev. Appl.* 15, 064015 (2021)

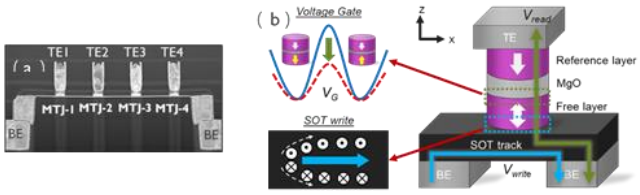

Fig. 1: (a) Lateral TEM cross-section view of the integrated MP-SOT device with four MTJ pillars. (b) Schematic of VCMA-assisted SOT switching.

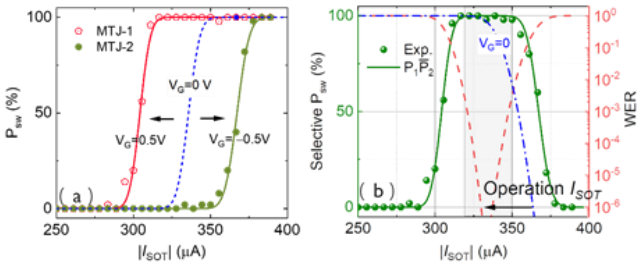

Fig. 2: (a) Measured P_{sw} of two individual bits on a shared SOT track. (b) The joint P_{sw} of selective write operations (switch P_1 and hold P_2).

6. Co-design of efficiently sampled probabilistic magnetic tunnel junctions for energy-efficient and hardware-aware variational inference

Christopher H. Bennett[1], Ravi Patel[1], Sam Liu[2], Nick Zogbi[2], Sapan Agarwal[1], Jean Anne Incorvia[2], and Patrick Xiao[1]

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[2]University of Texas at Austin

In our previous work [1], we have analyzed how in-plane magnetic tunnel junction (iMTJs) can be efficiently implemented into arrays that perform variational inference (VI) on-chip using a new circuit configuration. This design paves the way towards hardware VI systems that fulfill key uncertainty quantification (UQ) metrics while yielding between 10-100x energy advantages, depending on the size of the arrays. However, the sampling of the devices, which is expressive and takes place on the nanosecond time-scale [2], has not been fully optimized with respect to the VI training process nor the downstream hardware fabric. In particular, as iMTJs are sampled more rapidly, they accumulate sampling curves that are not smoothly Gaussian , but have a spiked shape (Fig. 1(a)). In this work, we demonstrate how various non-Gaussian sampling curves, derived from micromagnetic simulations of iMTJs, can be put in the loop with multi-objective optimization methods [3] to yield optimal neural network learning and architecture parameters. Once a variety of candidate hardware-aware VI networks have been trained, we can then evaluate the UQ performance of these networks to both test-set metrics (expected calibration error [4], as in Fig 1.(c)), as well as performance on truly out-of-distribution data. In addition, we consider how changes in material parameters, such as geometry and anisotropy, effect the downstream performance, and

put those changes in material parameters in the co-design loop.

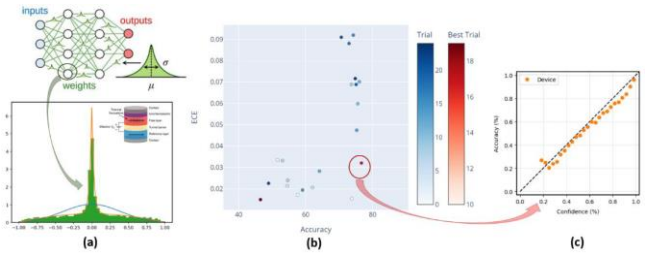

Fig1. (a) Schematic of an in-plane magnetic tunnel junction (MTJ) array sampling various nanodevices, with the non-Gaussian sampling shape at 10 nanoseconds shown (yellow curve) in contrast to standard (blue) surrogate posterior. (b) Multi-objective optimization performed on various learning and loss function parameters suggests the best configuration for the physical surrogate gradient curve (maximum accuracy, minimum ECE). (c) Winning trial on the CIFAR10 dataset is trained to completion. As shown ,the chosen instance has good calibration (model is neither over or underconfident over most of the test-set).

[1] Liu, Samuel, et al. "Bayesian neural networks using magnetic tunnel junction-based probabilistic in-memory computing." *Frontiers in Nanotechnology* 4 (2022): 1021943.
[2] Safranski, Christopher, et al. "Demonstration of nanosecond operation in stochastic magnetic tunnel junctions." *Nano letters* 21.5 (2021): 2040-2045.
[3] Ozaki, Yoshihiko, et al. "Multiobjective tree-structured parzen estimator for computationally expensive optimization problems." *Proceedings of the 2020 genetic and evolutionary computation conference*. 2020.
[4] Guo, Chuan, et al. "On calibration of modern neural networks." *International conference on machine learning*. PMLR, 2017.

7. Energy Efficient Nanomagnetic Devices for Non-volatile Memory and Hardware AI

Jayasimha Atulasimha

Virginia Commonwealth University

This poster will highlight our work on electrical control of magnetization in nanoscale magnets towards energy efficient and robust switching of perpendicular magnetic tunnel junctions (p-PTJs); as well as using nanomagnetic domain wall (DW) racetracks and quantized synaptic elements for deep neural networks and nanomagnetic oscillators for reservoir computing.

Non-volatile memory: We proposed skyrmion mediated electric field switching of perpendicular magnetic tunnel junctions (p-PTJs) [1, 2]. Towards this end, we have demonstrated creation and annihilation of skyrmions in films using only an electrical field [2] (Fig. 1a) based on voltage control of magnetic anisotropy (VCMA). Our simulations show such skyrmion mediated VCMA switching in p-MTJs is scalable to lateral dimensions below 20nm [3] while being robust to thermal noise and defects, offering memory density comparable to state-of-the-art.

Non-volatile quantized domain wall (DW) synapses for deep neural networks (DNNs): Recently, we showed that a domain wall racetrack device capable of providing only a limited number of memory states (nominally 5-state) along with stochastic variation within the states can be used efficiently as neural network synaptic weights in neuromorphic computing platform [3] (Fig. 1b). When used in in-situ training, such DW based DNN is useful as it can be trained with significantly lower number of weight updates and shows testing accuracy comparable with state-of-art.

Reservoir computing (RC): Skyrmion MTJs [5] and planar nanomagnets MTJs [6] can be used for low SWaP reservoir computing (Fig. 1c). Such systems, when appropriately designed, have the appropriate nonlinearity characterized by parity check (PC) and short-term memory (STM) capacities and can perform benchmark temporal data processing tasks.

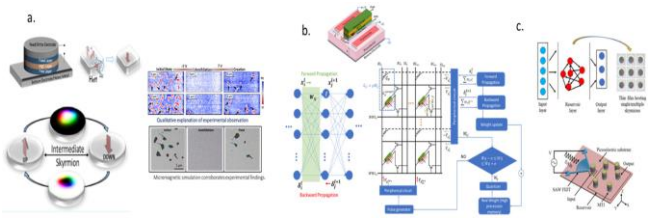

Figure 1: a. Skyrmion mediated switching of ferromagnet. Skyrmion creation and annihilation with the application of voltage. Figure reproduced from Ref. [1-2]. b. Learning of deep neural networks with limited state domain wall memory including device noise. Figure reproduced from Ref. [4]. c. Skyrmion and nanomagnet reservoir, the input excitation is voltage and surface acoustic wave respectively. Figure reproduced from Ref. [5-6].

[1] *ACS applied materials & interfaces*, **10**, 20 (2018): 17455-17462. doi: https://doi.org/10.1021/acsami.8b02791, [2] *Nature Electronics*, **3**, 9 (2020): 539-545. doi: https://doi.org/10.1038/s41928-020-0432-x, [3] *IEEE Transactions on Electron Devices*, **67**, 9 (2020): 3883-3888. doi: https://doi.org/10.1109/TED.2020.3011659, [4]. *IEEE Access*, **10** (2022): 84946 - 84959. doi: https://doi.org/10.1109/ACCESS.2022.3196688, [5] *Neuromorph. Comput. Eng.*, **2**, 4 (2022): 1-12. doi: https://doi.org/10.1088/2634-4386/aca178, [6] *Applied Physics Letters*, **121**,102402 (2022): 1-7. doi: https://doi.org/10.1063/5.0110769

8. P-Bit Design with Decoupled Stochastic and Control Paths for Enhanced Tunability

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[2]*Department of Electrical and Computer Engineering, University of California, Santa Barbara, Santa Barbara, CA, USA,*
[3]*Center for Advanced Materials, King Fahd University of Petroleum & Minerals, Dhahran, Saudi Arabia*

With the slowing pace of Moore's law, unconventional computing schemes are emerging rapidly to the field. Probabilistic computing which is a third branch of computing that combines elements of both quantum and digital computing [1], has surged again in the computing field with the introduction of probabilistic-bit (p-bit) based on a stochastic magnetic tunnel junction (sMTJ). P-bit was first proposed in 2017 [2] as a modified version of magnetic random-access memory (MRAM) technology, where the main difference is that the MTJ is made stochastic rather than being deterministic. It was evident that reported experimental implementations had narrow stochastic range (around 0.3V) [3-4], and only small p-bit networks were experimentally reported. Recently, a stochastic range of around 1V was reported in [5], but still the stochastic range can be further extended. Existing p-bit designs in the literature suffer from strong coupling between the stochastic and control (input) paths, as shown in Figs. 1(a-b), which restricts expanding the stochastic range and obstructs controlling the p-bit output accurately. The proposed p-bit modification (decoupled paths) is also inspired from MRAM technology based on MTJs. The evolution of MRAM technology has gone through many phases, starting from the magnetic core memory, reaching to the Spin Transfer Torque (STT-MRAM) and Spin Orbit Torque (SOT-MRAM). One major contribution in the MRAM field is the separation between the writing path and the reading path as it makes the memory device more reliable. Similarly, we try to demonstrate the impact of separating (decoupling) the stochastic path from the control (input) path for p-bits, as illustrated in Figs. 1(c-d). One valid implementation of the stochastic and control paths decoupling is a voltage divider composed of two stochastic devices as shown in Fig. 1(d). Such design makes the p-bit more tunable as the input voltage does not affect the stochastic response of the MTJ, where we can design the p-bit response to match any desired $\mathbf{tanh}(\boldsymbol{\beta V_{in}})$ as shown in Fig. 2(a). Also, it facilitates the fabrication process by eliminating the need for matching the MTJ with the NMOS. Moreover, the stochastic range of the new design is beyond what is reported in the literature as shown in Fig. 2(b), where we analytically derive the stochastic range of the new design and plot it against the reported experimental implementations.

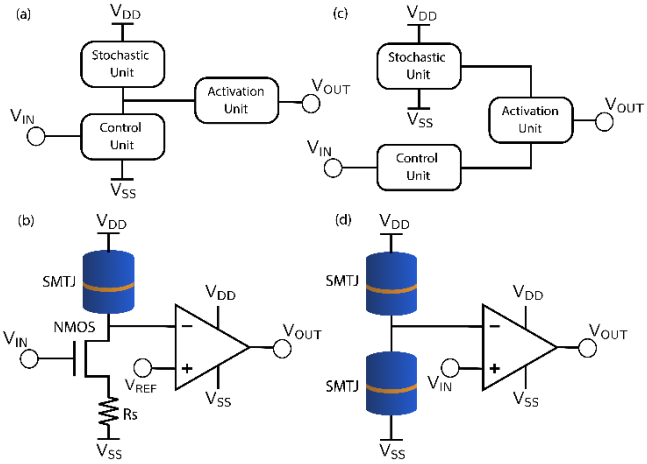

Fig. 1. Stochastic path and control path coupling. (a-b) Conventional probabilistic bit (p-bit) structure where the stochastic and control paths are coupled. (c-d) Proposed modification by decoupling the stochastic path from the control path, which also decouples the design of these two paths.

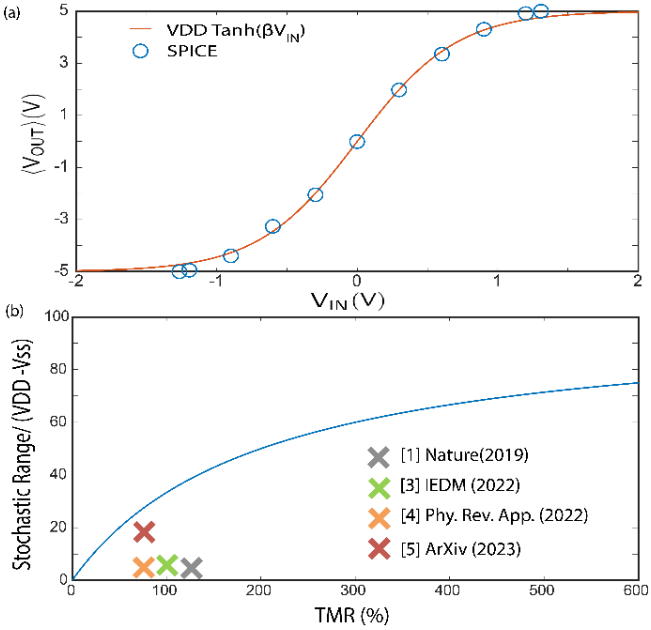

Fig. 2. (a) Mapping the average stochastic response of the voltage divider implementation of the p-bit (simulation) to the tanh function. The tanh function was scaled by V_{DD} so that the two plots would have equal limits. (b) Analytical limit for the voltage divider decoupled design, where bigger stochastic range achieved at high TMR values. All experimental implementations of p-bits are below the limit.

[1] Borders, William A., et al. "Integer factorization using stochastic magnetic tunnel junctions." *Nature 573.7774* (2019): 390-393, **[2]** Camsari, Kerem Yunus, Sayeef Salahuddin, and Supriyo Datta. "Implementing p-bits with embedded MTJ." *IEEE Electron Device Letters* 38.12 (2017): 1767-1770, **[3]** Grimaldi, Andrea, et al. "Experimental evaluation of simulated quantum annealing with MTJ-augmented p-bits." 2022 *International Electron Devices Meeting (IEDM). IEEE*, 2022, **[4]** Kaiser, Jan, et al. "Hardware-aware

in situ learning based on stochastic magnetic tunnel junctions." *Physical Review Applied* 17.1 (2022): 014016, **[5]** Kobayashi, Keito, et al. "CMOS+ stochastic nanomagnets: heterogeneous computers for probabilistic inference and learning." *arXiv preprint arXiv:2304.05949* (2023).

9. Domain Wall Magnetic Tunnel Junction Logic Using Voltage Controlled Magnetic Anisotropy

Nicholas Zogbi[1], Jean Anne Incorvia[1], and Tianyao Patrick Xiao[2]
[1]University of Texas at Austin, [2]Sandia National Laboratories

Magnetic computing devices have shown great promise to be used complementary with CMOS devices, since they can theoretically switch with orders of magnitude less voltage. Magnetic logic devices can be created using three-terminal domain wall magnetic tunnel junctions (DW-MTJ) [1]. Data is encoded based on the position of the DW, which also forms the free layer of the MTJ. This read current is also used to concatenate logic: if another device is connected to the MTJ and the amplitude of the current is strong enough, the DW of the connected device will propagate.

However, challenges remain for the reliability of DW-MTJ logic. Previous iterations relied on DW inertia as a way to complete a read operation. This creates errors when conducting multiple reads and writes on a single device due to inconsistent positions of the DW. In addition to reliability issues, implementing different logic functions required modifying the device footprint. Here, instead of relying on DW inertia, we incorporate voltage controlled magnetic anisotropy (VCMA) electrodes into the device (Fig. 1) to draw the DW to the lower anisotropy points. We also design the device for a constant footprint vs. logic operation and fanout [2]. Using the micromagnetic simulation software MuMax3, we show improved reliability, with 100% accuracy at various TMRs when conducting multiple reads and writes. We then simulate a 256×256 systolic array of DW-MTJs and benchmark against Google's TPUv1. The results show that using a fine-grained pipelining technique, pipelining of logic instead of instructions, the efficiency and throughput of the systolic array are on par with state-of-the-art CMOS accelerators for neural network inference. These results show that the newly designed nonvolatile spintronic logic devices can be used for edge computing applications while offering robustness under extreme environments.

SNL is managed and operated by NTESS under DOE NNSA contract DE-NA0003525.

[1] M. Alamdar *et al.*, "Domain wall-magnetic tunnel junction spin–orbit torque devices and circuits for in-memory computing," *Applied Physics Letters,* vol. 118, no. 11, 2021, doi: 10.1063/5.0038521.
[2] N. Zogbi *et al.*, "Parallel Matrix Multiplication Using Voltage-Controlled Magnetic Anisotropy Domain Wall Logic," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits,* vol. 9, no. 1, pp. 65-73, 2023, doi: 10.1109/jxcdc.2023.3266441.

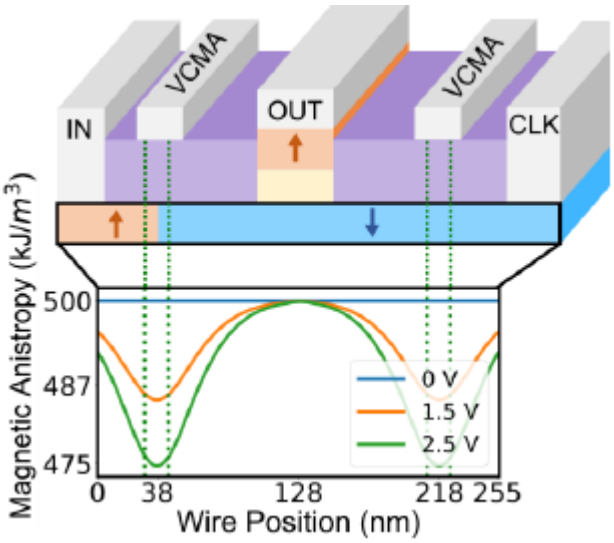

Fig. 1: DW-MTJ logic device schematic with magnetization shown by the arrows. The VCMA electrodes apply voltage through the oxide, below is the calculated magnetic anisotropy at various applied voltages.

10. Energy Efficient Nanomagnetic Devices for Non-volatile Memory and Hardware AI

Walid Al Misba, Md Mahadi Rajib*, Md Fahim F. Chowdhury*, Muhammad Sabbir Alam*, Austin Roe*, Dhritiman Bhattacharya*, J. Atulasimha*,**,#*

Mechanical and Nuclear Engineering Dept., Electrical and Computer Engineering Dept.** , Physics Dept.# ,Virginia Commonwealth University*
Collaborators (for work presented here): K. L. Wang Group, UCLA; J. S. Friedman Group, UT Dallas; Damien Querlioz, CNRS, Université Paris-Saclay, B.K. Kaushik Group, IIT Roorke, M. Manic Group, VCU

11. Pulse Width Dependence of Switching Characteristics for Magnetic Tunnel Junction

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In some MTJs, intermediate (IM) states have been reported to appear between antiparallel (AP) and parallel (P) states[1-3]. Therefore, we investigated the switching characteristics of MTJs with SiN sidewall shown in Fig. 1. The pulse with voltage from ±0.15 V to ±0.6 V were applied to the MTJ, and the pulse width varied from 100 ns to 1 µs. After applying the pulse, the current was measured at 0.06 V. Figures 2 and 3 show the resistance at reading voltage of 0.06V (R@0.06V)for 120nm size and 300nm size MTJ. These data are extracted from ±0.3 to ±0.5 V from all measured data. The results show that IM states appear both 120nm size and 300nm size MTJ. Furthermore, the number of IM state increases with an increase of the MTJ size. It is considered that there are multiple regions with different switching characteristics in the free layer and the resistance depends on the number of regions where magnetization change occurs.

The relationship between switching voltage and write error for each pulse width from 100 ns to 1 µs was investigated, and then the write error rate (WER) increase with decrease of the pulse width or switching voltages. Therefore, at narrow pulse widths, high voltages are required to eliminate the WER. MTJs with IM states require higher voltages or wider pulse widths than MTJs without IM states for no-error switching, and it causes high power consumption.

[1]C. Watanabe, et al., Special MRAM poster session at IEDM 2022, ID1. [2] Y. Miyazaki, et al., Ext. Abst. of SSDM 2023, p. 483. [3]L. Wu, et al., IEEE Trans. Comput. 71, 2219 (2022).

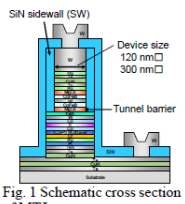

Fig. 1 Schematic cross section of MTJ structure

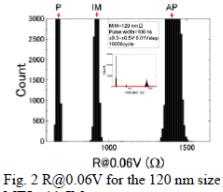

Fig. 2 R@0.06V for the 120 nm size MTJ with IM state.

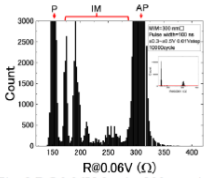

Fig. 3 R@0.06V for the 300 nm size MTJ with IM state.

12. Unified Modeling of Ultra-Scaled STT-MRAM Cells: Harnessing Parasitic Effects for Enhanced Data Storage Dynamics

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Magnetoresistive Random Access Memory (MRAM) stands out as a nonvolatile memory solution with enhanced endurance and retention over traditional flash memory, predominantly attributed to its Magnetic Tunnel Junction (MTJ). This MTJ comprises a composite Free Layer (FL) and a Reference Layer (RL) separated by a MgO Tunnel Barrier (TB). With added MgO layers [1] and elongated FLs [2], the MTJ enhances perpendicular magnetic anisotropy, thereby shrinking the cell's footprint [3].

The design and optimization of such advanced, single digit-nanometer diameter shape-anisotropy MRAM cells necessitate a precise understanding of spin currents and torques, especially in MTJs with extended FLs and RLs.

Our research has pioneered a comprehensive modeling approach using a three-dimensional finite element method to address this need. This method encapsulates all significant physical phenomena vital for ultra-scaled MRAM cells. It integrates the drift-diffusion methodology — previously successful in modeling nanoscale metallic spin valves — into the context of MTJs. We modeled the TB as a poor conductor, where its local conductivity is influenced by the relative magnetization orientation, effectively capturing the dependence of current flow on the magnetization state. Appropriate boundary conditions at the TB interfaces were introduced to accommodate the interfacial spin current polarization and, therefore, reproduce the angular dependence of the torque [4].

A critical discovery through our simulations is the highly nonuniform magnetization profile during switching in elongated FLs of ultra-scaled MRAM cells. This nonuniformity leads to domain wall formations, which experience additional torques, traditionally modeled using the expression by Zhang and Li. Our findings reveal that, given an MTJ's presence, the Slonczewski and Zhang-Li torques are interconnected. A unified approach to MTJ and FL magnetization texture is essential for accurately portraying the torque in elongated magnetic layers.

Moreover, our simulations delve into the intricate magnetization dynamics in elongated cells with multiple TBs. Our model's predictions consistently align with recent experimental results for ultra-scaled MRAM cells. A particularly intriguing observation during our study was the sequential switching of a FL containing two ferromagnetic segments divided by a tunnel junction. The switching from a parallel to an anti-parallel configuration revealed a distinctive back-hopping phenomenon, typically deemed parasitic [5]. We innovatively leveraged this effect to illustrate a multi-level operation in ultra-scaled MRAM cells, introducing a departure from the conventional binary MRAM operation. Instead, our revelations highlight a cyclic which switching spans four distinct states of the FL under a consistent current polarity.

Our integrated modeling approach offers a blueprint for the evolution of ultra-scaled MRAM cells. Harnessing cyclic switching through what was once considered a parasitic effect could herald a significant leap in MRAM technology. Such advancements augur well for elevating data storage capacities and emphasize MRAM's prospective role in the next-generation electronic apparatus.

[1] H. Sato et al., IEEE T Magn., vol. 49, pp. 4437-4440, 2013, [2] K. Nishioka et al., IEEE T Electron Dev., vol. 67, pp. 995-1000, 2020, [3] B. Jinnai et al., Proc. of the IEDM, pp. 24.6.1-24.6.4, 2020, [4] S. Fiorentini et al., Sci. Rep., vol. 12, no. 20958, 2022, [5] C. Abert et al., Phys. Rev. Appl., vol. 9, no. 054010, 2018.

13. MRAM / CMOS hybridization to secure cryptographic algorithms

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The increasing use of Internet of Things (IoT) objects is associated with a necessity to develop low-power and secure circuits. Lightweight Cryptography algorithms are used to secure the communications of these connected objects at a limited power consumption. These algorithms need to be securely implemented to withstand physical attacks. However, the proposed countermeasures often consume significant energy. As a result of its low energy requirements, it becomes possible to hybridize STT-MRAM devices with CMOS and construct non-volatile logic for connected devices that have to wake up on event and retain data storage when the circuit is sporadically powered off. In this context, this poster details the two main parts of the MISTRAL project:

- the design of an hybrid CMOS/ STT-MRAM ASCON cipher, selected by the National Institute of Standards and Technology (NIST) for future standardization of the LWC. This implementation (layout shown in Fig. 1) provides energy saving ranging from 19% to 54% for an area overhead of 5.5%. Several attack scenarios have shown that the hybrid implementation does not pave the way to new critical vulnerabilities.
- the STT-MRAM bitcell vulnerability analysis under laser attack. The MTJs have been exposed to a 1064nm laser irradiation (Fig. 2), highlighting a reading current variation during the laser shots. A possible switch from Anti-Parallel to Parallel state is also demonstrated. We correlate this MRAM behavior under laser attack to a thermal effect. These effects are included in the full algorithm design and simulation to implement countermeasures.

The MISTRAL project, coordinated by Mines Saint-Etienne in Gardanne, in collaboration with CEA, Spintec and IM2NP, is funded by the National Research Agency (Grant ANR-19-CE39-0010) with the aim of securing Lightweight Cryptography (LWC) algorithms through CMOS/STT-MRAM hybridization.

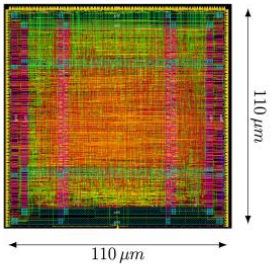

Fig. 1 Layout of ASCON hybrid circuit.

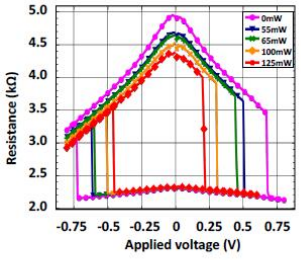

Fig. 2 Laser power variation on the quasi-static R-V characteristics during the programming cycle.

14. Enhancing the performance of magnetic tunnel junctions using He^+ ion irradiation

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We have developed a new manufacturing process based on He+ ion irradiation to tailor the structural properties of ultra-thin magnetic materials at atomic level and enhance their performance. The utilization of light ions provides the precise control of inter-atomic displacements through low energy transfer. The key feature of the technology is the post-growth control at the atomic scale of structural properties and the related magnetic properties. When realized through a mask this technology allows lateral modulation of magnetic properties without any physical etching.
In this poster, we will demonstrate that He^+ ion irradiation of Magnetic Tunnel Junctions can enhance the performance of MRAM, magnetic sensor and neuromorphic computing. We will also introduce Spin-ion's process adoption plan for customers including ion beam services, ion beam facilities and IP licencing.

15. A quantum sensing metrology for magnetic memories

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Magnetic random access memory (MRAM) is a leading emergent memory technology that is poised to replace current non-volatile memory technologies such as eFlash. However, the scaling of MRAM technologies is heavily affected by device-to-device variability rooted in the stochastic nature of the MRAM writing process into nanoscale magnetic layers. Here, we introduce a non-contact metrology technique deploying Scanning NV Magnetometry (SNVM) to investigate MRAM performance at the individual bit level. We demonstrate magnetic reversal characterization in individual, < 60 nm sized bits, to extract key magnetic properties, thermal stability, and switching statistics, and thereby gauge bit-to-bit uniformity. We showcase the performance of our method by benchmarking two distinct bit etching processes immediately after pattern formation. Unlike previous methods, our approach unveils marked differences in switching behavior of fully contacted MRAM devices stemming from these processes. Our findings highlight the potential of nanoscale quantum sensing of MRAM devices for early-stage screening in the processing line, paving the way for future incorporation of this nanoscale characterization tool in the semiconductor industry.